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Analysis and Implementation of Low-Power Double Tail Comparator

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Abstract: Comparators are the fundamental circuit elements in Analog to digital converters. Efficient design of these comparators with optimizing factors like operational frequency, power consumed per conversion, low voltage input rate, has become a challenge. In this paper, an analysis is presented on single tail comparator, conventional double tail comparator & double tail comparator with reduced leakage power. This presented third circuit particularly carries weight, since the drastic scaling down of transistor size which leads us to consider sub- threshold power leakage. For this we have shown a conventional dynamic double tail comparator using CMOS inverter. The simulation results consolidate the power leakage levels reduced in the proposed circuit. The time delay of final circuit is 2.5ns and the power consumed is 4.5uW.The simulation results are shown in 180nm Technology using Cadence.

Keywords: Double tail comparator, dynamic comparator, reduced leakage, sub-threshold region.

I. INTRODUCTION

One of the most important basic building blocks in analog circuits is the comparator. The function of a CMOS comparator is to compare an input signal with a reference voltage and produces binary signal output. Comparator uses back to back cross coupled inverters to convert the voltage into digital output in a short period of time. The performance of the comparator plays an important role in realizing of efficient power, cost and design parameters.

This is especially difficult because of the minute mismatches, low-voltages in ultra deep semiconductors CMOS technology. In the technological advancement in this domain threshold voltage have been not scaled as much when compared to supply voltages [1]. Hence designing high speed circuits is more challenging. To get high speed, larger transistors are required to compensate the reduction of supply voltage. The comparator design is slightly modified in order to reduce the leakage power which further reduces the total power and delay of the circuit. As the three models in the paper are covered you can see the reduction of power consumed. Furthermore we can analyse the other factors like kick back noise, random decision noise etc..if we wish to compare them as well for detailed analyses.

II. SINGLE TAIL COMPARATOR

It is first model among the dynamic comparators which utilised single current stabilizer (i.e. nmos in this case) which is controlled by clock. This circuit has advantages of high input impedance and absence of static power consumption. The comparator works in two essential ways, they are comparison phase and reset phase. These will be elaborated in the proceeding section.

III. OPERATION

There are many papers presenting the detail analysis of the present circuit. So we shall discuss briefly the two cases that occur.

When Clk=0, this circuit operates in reset phase. In this phase, TAIL transistor get off and reset transistors pull both output nodes Out n and Out p to V_{DD} to have a valid logical level during this phase.

$$t_{delay} = t_0 + = 2\frac{C_L|V_{thp}|}{I_{tail}} + \frac{C_L}{g_{m,eff}} \cdot \ln\left(\frac{V_{DD}}{4|V_{thp}|\Delta V_{in}}\sqrt{\frac{I_{tail}}{\beta_{1,2}}}\right)$$

When CLK = V_{DD}, this circuit operates in comparison phase, transistors Q1 and Q4 are off, and M_{tail} is on. Outp, Outn which had been pre-charged to V_{DD} and start to discharge with different discharging rates depending on the corresponding input voltage (INN/INP).

Let us consider the case where VINP > VINN, Outp discharges faster than Outn, when Outp falls down to (V_{DD}-V_{thpmos}) ,the corresponding pMOS transistor (Q2) will turn on by initiating the positive feedback mechanism (latch regeneration) caused by inverters connected back-to-back (Q5, Q2 and Q6, Q3). If VINP < VINN, the circuits works vice versa [2].

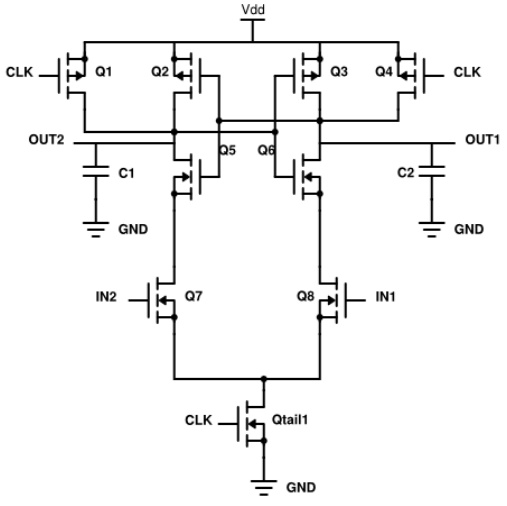

Fig 1.Schematic diagram of the conventional dynamic comparator

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This circuit has advantages like high input impedance, high rail-rail swing, low static power consumption and immunity against noise cross-over. Since parasitic capacitance doesn't cause a change to switching speeds of output node, so it is possible to use i/p transistors and reduce offset.

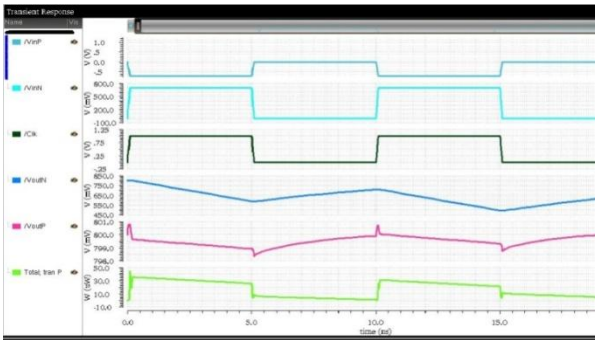

Fig.2. Transient simulations of the conventional dynamic comparator forinput voltage difference of ΔV_d= 0.7 V, and VDD = 0.8 V.

IV. CONVENTIONAL DOUBLE TAIL COMPARATOR

This design has less number of stacked transistors. Latching and difference amplifier are separated in the terms of functionality and power usage during the 'Comparison phase' and are removed of supply source in 'Reset phase'. This not only allows us to save power but also the current control of latching and difference amplifier are done independently.

V. OPERATION

In reset phase i.e. CLK=0 Q7 and Q8 are pulled upto V_{DD}. Which are connected to output nodes and leads Q3 and Q6 to discharge to ground .Whereas during decision making phase i.e.CLK=V_{DD} Q7and Q8 switches off leading $f_p$and $f_n$to discharge a rate decided by $I_{Mtail1}/C_{fn(p)}$. The undecided stated formed in between transitions of voltage i.e. $V_{fn(p)}$ passes through the cross coupled inverters and acts as a cut between input and output[1][3].

Similar to the conventional double taildynamic comparator, the delay of this comparator comprises two main parts, t_0 and t_{latch}. The delay t_0 represents the load capacitance C_{Lout} (at the latch stage output nodes, Outnand Outp) until the first n-channel transistor (Q4/Q6) turns on, after which the latch regeneration starts; thus t_0 is obtained

From:

$$t_0 = \frac{V_{Thn}\, C_{Lout}}{I_{B1}} \approx 2\frac{V_{Thn}\, C_{Lout}}{I_{tail\,2}}$$

Where I_{B1} is the drain current of the Q4 and is approximately equal to the half of the tail current (I_{tail2}). After the first n-channel transistor of the latch turns on (for instance, Q4), the corresponding output will be discharged to the ground, leading front p-channel transistor to turn on, charging another output (Outp) to the supply voltage (V_{DD}). The regeneration time (t_{latch}) is achieved. For the initial output voltage difference at time t_0,[2]ΔV_0 we have

$$\Delta V_0 = \left|V_{outp}\,(t = t_0) - V_{outn}\,(t = t_0)\right| = V_{Thn} - \frac{I_{B2}\, t_0}{C_{Lout}} = V_{Thn}\left(1 - \frac{I_{B2}}{I_{B1}}\right)$$

Where I_{B1} and I_{B2} are the currents of the side branch and can be rewritten as follows:

$$\Delta V_0 = V_{Thn}\frac{\Delta I_{latch}}{I_{B1}} \approx 2V_{Thn}\frac{\Delta I_{latch}}{I_{tail\,2}} = 2V_{Thn}\frac{g_{mR1,2}}{I_{tail\,2}}\Delta V_{fn/fp}$$

$$\Delta V_{fn/fp} = \left|V_{fn}(t = t_0) - V_{fp}(t = t_0)\right| = t_0 \cdot \frac{I_{N1} - I_{N2}}{C_{L,fn(p)}} = t_0 \cdot \frac{g_{m1,2}\Delta V_{in}}{C_{L,fn(p)}}$$

$$\Delta V_0 = 2V_{Thn}\frac{g_{mR1,2}}{I_{tail\,2}}\Delta V_{fn/fp} = \left(\frac{2V_{Thn}}{I_{tail\,2}}\right)^2 \cdot \frac{C_{Lout}}{C_{L,fn(p)}} \cdot g_{mR1,2}\, g_{m1,2}\Delta V_{in}$$

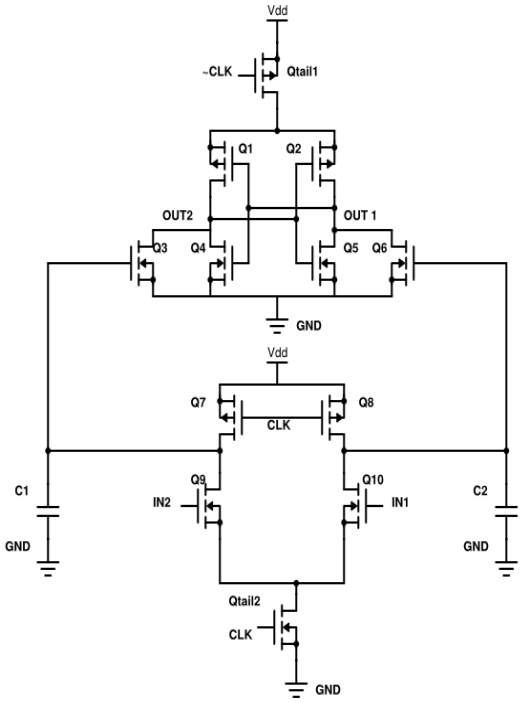

Fig. 3.Schematic diagram of the conventional double-tail dynamic comparator

Therefore delay can be calculated by using the derived formula that is

$$t_{delay} = t_0 + t_{latch} = 2\frac{V_{Thn}C_{Lout}}{I_{tail\,2}} + \frac{C_{Lout}}{g_{m,eff}} \cdot ln\left(\frac{V_{DD}/2}{\Delta V_0}\right) = 2\frac{V_{Thn}C_{Lout}}{I_{tail\,2}} + \frac{C_{Lout}}{g_{m,eff}} \cdot ln\left(\frac{V_{DD} \cdot I_{tail\,2}^2 \cdot C_{Lfn(p)}}{8V_{Thn}^2 \cdot C_{Lout}\, gmR\,1,2\, gm\,1,2\Delta V_{in}}\right)$$

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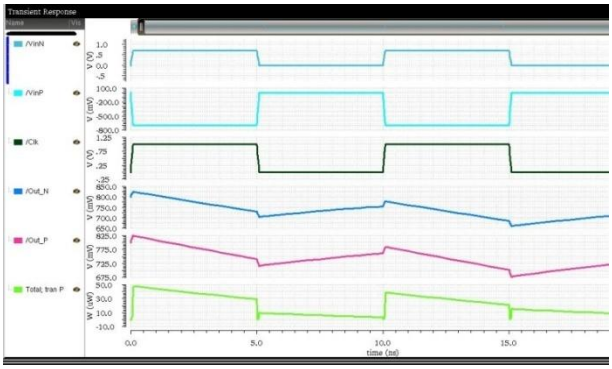

Fig.3. Transient simulations of the conventional double-tail dynamic comparator for input voltage difference of ΔV_d= 0.7 V, and VDD = 0.8 V.

These are the following key points that can be deduced from the above derivation.

- The voltage output difference at first output stage is affecting the final output voltage difference drastically. Therefore the delay would be reduced immensely when first stage output voltage difference is increased.
- The intermediate transistors consume power during reset phase and seldom have utility in reducing transconductance in comparison phase.

VI. SUB-THRESHOLD CONDUCTION

As technology scales down, the size of transistors has reduced significantly. The number of transistors on chip will thus increase to improve the performance of circuits. In order to sustain the characteristics of an MOS. the supply voltage, being one of the critical parameters, has also been reduced accordingly. Therefore the threshold voltage is also scaled down at the same rate as the supply voltage in order to maintain the transistor switching speed. As a result, leakage currents increase drastically with each technology generation. As the leakage current increases faster, it will become more and more proportional to the total power dissipation.

$$PLEAK = I_{LEAK} * V_{DD}$$

To reduce total leakage in nanoscale circuits, some new techniques have to be developed to reduce the sub threshold leakage especially for chips that are used in portable systems which are power constrained. The leakage current consists of reverse bias diode currents and Sub-threshold current. The reverse bias current is due to the stored charge between the drain and bulk of active transistors while the Sub-threshold current is due to the carrier diffusion. Hence, in this paper conventional CMOS inverter based approach is used to reduce the Sub-threshold leakage power.

VII. PROPOSED REDUCED LEAKAGE POWER DOUBLE TAIL COMPARATOR

The amplifier circuit is modified according to the inverter logic. The inverter logic which reduces the leakage. Here, two inverters are used. The inputs are applied to two inverters and the outputs are connected to an active load. The circuit will be used in our double tail comparator structure [4][3]. The differential amplifier will be modified with this inverter logic. The output will be applied to the latch for regeneration.

Hence, out1 pulls up to VDD. When out1 goes to VDD, the transistor Q1 will be off which remains out2 at ground. By using this approaches the Sub-threshold leakage and hence the total power will be reduced. The simulation results prove the reduction. Here in the differential amplifier inverters are used which are series transistors.

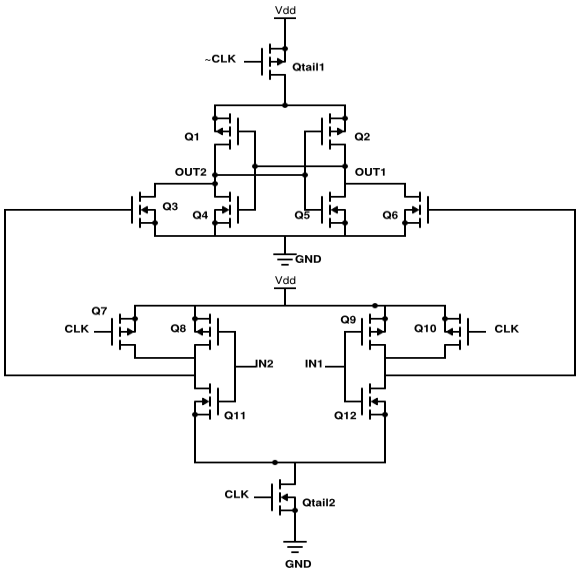

Fig.4. Schematic diagram of the optimised double-tail dynamic comparator

Fig.3. Transient simulations of the proposed optimised double-tail dynamic comparator for input voltage difference of ΔV_d= 0.7 V, and V_{DD}= 0.8 V.

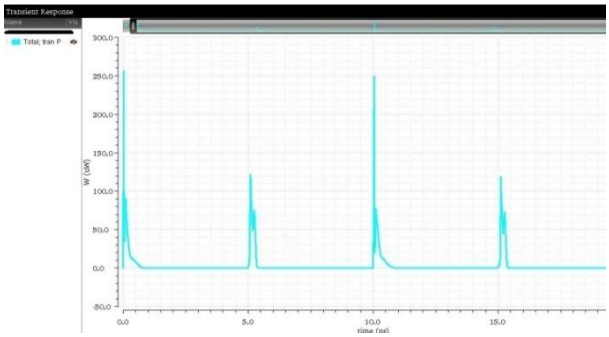

Fig.4. power dissipation of the proposed optimised double-tail dynamic comparator

Hence, the trans-conductance of the total circuit increases which reduces the total delay of the circuit. Hence, by using this CMOS inverter approach the total power and delay can be reduced. The simulation results show the reduction in both power and delay.

VIII. RESULTS

TABLE I. POWER CONSUMPTION

S. No	Comparator type	Power consumed in μW
1	Conventional single tail comparator	21.90uW
2	Conventional double tail comparator	34.73uW
3	Reduced leakage-power of proposed double tail dynamic comparator	3.2uW

IX. CONCLUSION

In this paper we have discussed the power consumption and delay analysis of dynamic comparators along with reduced leakage power circuit and a comprehensive output is shown along with simulation results. This analysis is done in 180nm CMOS technology using Cadence software

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